AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 10, line 16, with the following amended paragraph:

The amplitude restricting circuit 7 restricts the amplitude so that the absolute value of the input high-frequency signal Sf does not exceed the amplitude-restricting signal Si, and supplies the amplitude-restricted high-frequency signal Sj to the adder 8. Fig. 6 shows details of the amplitude restricting circuit 7. As illustrated, the amplitude restricting circuit 7 has an input terminal 701 for receiving the output signal Sf of the high-frequency extracting circuit 5, an input terminal 702 for receiving the output signal Si of the amplitude-restricting signal generator 6, an absolute value circuit 71 for determining the absolute value of the signal Sf, and a comparator 72 for comparing the output signal of the absolute value circuit 71 with the signal Si, a sign inverting circuit 73 for inverting the sign of the signal Si, a first selector 74, ~~a first selector 74,~~ a second selector 75, and an output terminal 203.